

DESIGN OF REVERSIBLE TECHNOLOGY BASED PARITY GENERATOR

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ABSTRACT

Current generation processors based on CMOS technology are facing heat dissipation problem. Reversible technology overcome this problem. Logical and physical reversibility based gate primitives can be implemented using Quantum-dot Cellular Automata (QCA) based nanotechnology. In this paper, reversible based gates are implemented using QCA technology. Further, parity generator is developed with the help of reversible gates. The basic parameters like area, power are calculated for the proposed reversible parity generator.

Keywords—Feynman Gate, Toffoli Gate, Peres Gate, Fredkin Gate, quantum cost, garbage output, power dissipation and Quantum Cell Automata

I. INTRODUCTION

Energy loss is an important consideration in digital circuit design, also known as circuit synthesis. The loss of information is associated with laws of physics describing that one bit of information lost dissipates $kT \ln 2$ of energy, where k is Boltzmann's constant and T is the temperature of the system. Reversibility in computing implies that information about the computational states should never be lost. The reversible logic is either physical reversible or logical reversible. Reversibility in computing implies that no information about the computational states can never be lost, so we can recover any earlier stage by computing backward or uncomputing the results. This is known as logical reversibility. The benefits of logical reversibility can be gained only after employing physical reversibility. Physical reversibility is a process that dissipates no heat in terms of wastage of energy. Various parameters of reversible logic gates are used to design the work. A Reversible logic gate is an n -input n -output logic function in which there is a one-to-one correspondence between the inputs and the outputs. A reversible gate is also defined as a objective Boolean function from n to n values. These reversible circuit elements gradually move the charge from one node to next as there is no flow of current in the circuit and hence no changing of voltage levels. With every transition, this will lead to a loss of a minute amount of energy transition. Digital logic designs can be drastically modified with reversible computing.

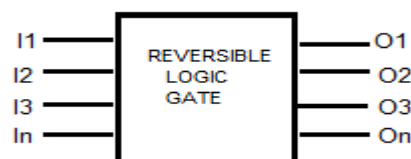


Fig.1. Symbol of Reversible logic gate with $n \times n$ input and output

To achieve an optimized circuit following points must be considered.

- [1] Garbage outputs must be minimum.
- [2] Loops or feedbacks are not permitted.
- [3] Minimum quantum cost.
- [4] Fan-out is not permitted.

II. LITERATURE SURVEY

In 1961, R.Landauer described that the logical irreversibility is associated with physical irreversibility and requires a minimal heat generation per machine cycle. For irreversible logic computations, each bit of information lost generates $kT \log 2$ joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. In a conventional system, the millions of gates used to perform logical operations. The Author proved that heat dissipation avoidable if the system made reversible.

In 1973, C.H.Bennett described that if a computation is carried out in Reversible logic zero energy dissipation is possible, as the amount of energy dissipated in a system is directly related to the number of bits erased during computation. The design that does not result in information loss is irreversible. A set of reversible gates is needed to design the reversible circuit. Reversible gate can generate a unique output vector from each input vector and vice versa.

Reversible logic has shown potential to have extensive applications in emerging technologies such as quantum computing, optical computing, quantum dot cellular automata as well as ultra low power VLSI circuits. Its output is same number of input and it used one to one mapping. In normal circuit we can't retrieve errors of output so that we made circuit by using reversible logic circuits. From that we are able to find error and so that we can able to solve error easily. In this paper we have represented detail of QCA and implementation of simple gates and Reversible logic gates with simulation result using QCA Designer.

QCA

Quantum dot cellular automata (QCA) is one of the emerging nanotechnologies that exhibit a small feature size, high clock frequency, and ultra low-power consumption [1], QCA provides an alternative way of computation, in which the logic states ("0" and "1") are defined by the positions of the electrons. Due to the significant error rates in nanoscale manufacturing and nanotechnologies, including the QCA, there is a critical need to maintain extremely low device error rates [3].

QCA CELL

In QCA data transfers because the electrons align themselves in the cell. The cell is of limited area which has area of few square nanometers. Potential wells are present in the QCA cells which are placed on four corners of the cell. Each cell has two electrons which are placed in either of the diagonal potential wells. This is because the coulomb forces will be applied to the electrons and they will try to repel each other resulting, in them being placed at the diagonal ends. The potential wells are connected to each other via the electron tunnel junction. These junctions can be activated when a clock signal arrives and opens the junctions for electrons to travel [2].

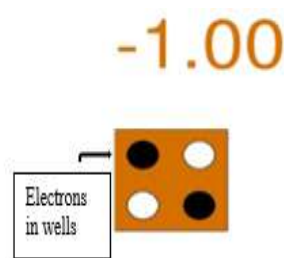


Fig 2.1.1 Binary 0



Fig 2.1.2 Binary 1

QCA WIRE

The fundamental unit of any electronic circuit is a wire. Without it, the transfer of data is not possible. In QCA, multiple cells when placed horizontally form a wire. In the wire, the data flows due to the coulombic interaction among the electrons. For the information to flow the electrons must be in the position as shown in Fig 3

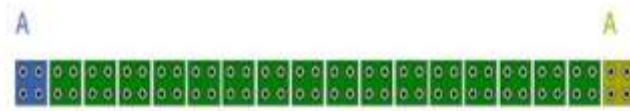


Fig 3 QCA Wire

MAJORITY VOTER (MV)

In QCA, a majority voter is designed with the help of five QCA cells. Three of those cells work as inputs, one cell as output and one as a center cell. The coulombic interaction among them results in the output being the majority of the three input cells. Let the input cells be A, B, C and the output cell be F. So the output $F = \text{Maj}(A,B,C) = A.B + B.C + C.A$.

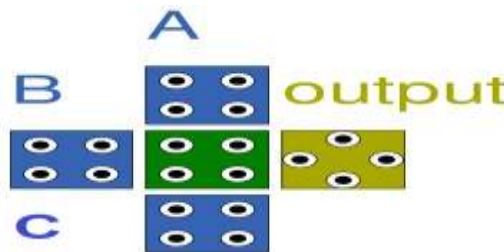


Fig.4. Majority Voter

III. DESIGN OF REVERSIBLE LOGIC GATES

There are some basic reversible gates mention below

- 1) NOT GATE
- 2) FEYNMAN GATE
- 3) TOFFOLI GATE
- 4) FREDKIN GATE
- 5) PERES GATE

1. NOT GATE

A Not gate is a 1×1 reversible gate is shown in Fig. 2. The input is A and the output is $B = A'$ which is reversible.

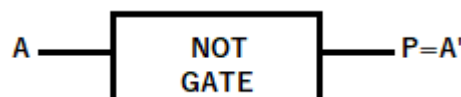


Fig .5 Reversible Not Gate Block Diagram

Table 1. Truth Table of NOT Gate

Input	Output
A	P
0	1
1	0

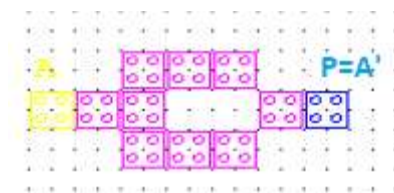


Fig. 6 Inverter in QCA Designer

2. FEYNMAN GATE

Feynman gate was given by Richard Feynman in 1982, which is a 2×2 reversible gate. Feynman gate can perform negation operation but in controlled way and it is also known as Controlled NOT Gate. If two line are A and B, the first line A is known as CONTROL line and second line B is known as TARGET line. Operation on target line is negation and only performed when control line is set otherwise no operation on target line is observed.

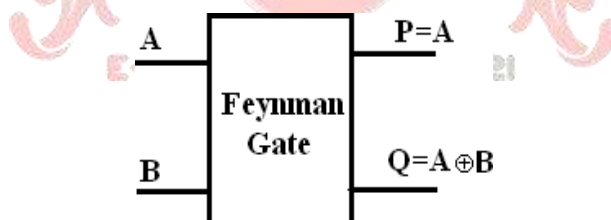


Fig. 7. Feynman Gate – 2×2 gate

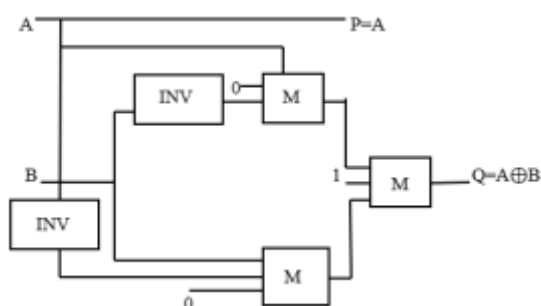


Fig. 8. Block Diagram of Feynman Gate

Table 2. Truth Table of Feynman Gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

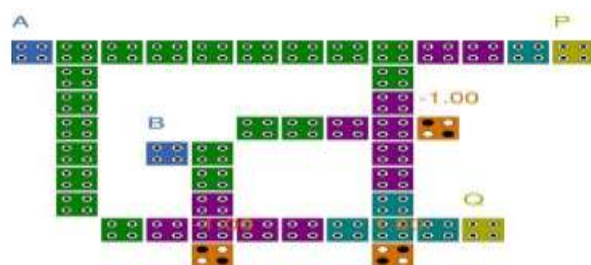


Fig. 9. Feynman Gate in QCA Designer

3. TOFFOLI GATE

In 1982 Toffoli give a new gate called Toffoli gate. It is a 3×3 gate and can be generalized up to $n \times n$ size. As per definition target line flips when all control lines are set.

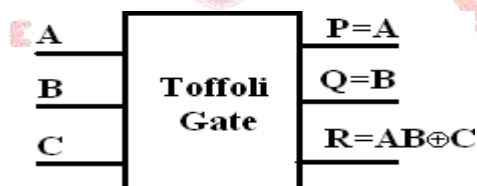


Fig. 10. Toffoli Gate – 3×3 gate

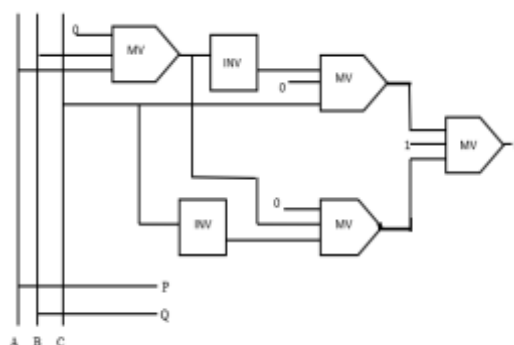


Fig.11. Block Diagram of Toffoli Gate

Table 3. Truth Table of Toffoli Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

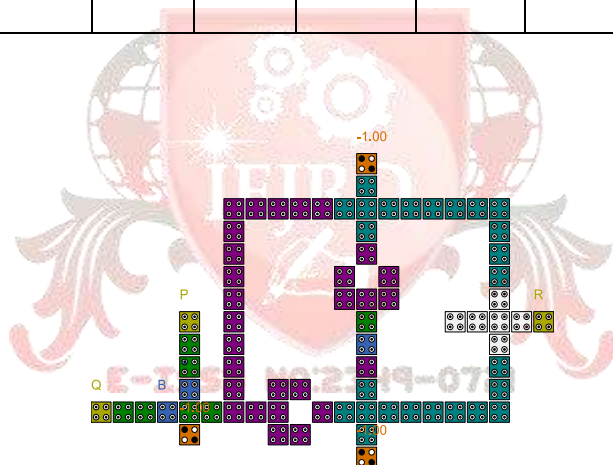


Fig. 12. Toffoli Gate in QCA Designer

4. FREDKIN GATE

In 1982 Edward Fredkin and Tommaso Toffoli proposed a new gate called 3×3 Fredkin Gate which is further generalized up to n lines. If C=0 3×3 Fredkin gate will swap the values of A and B.

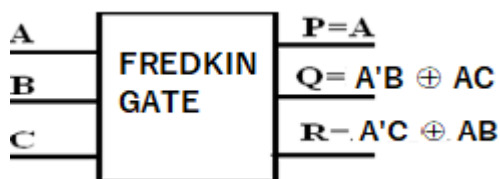


Fig. 13. Fredkin Gate – 3*3 gate

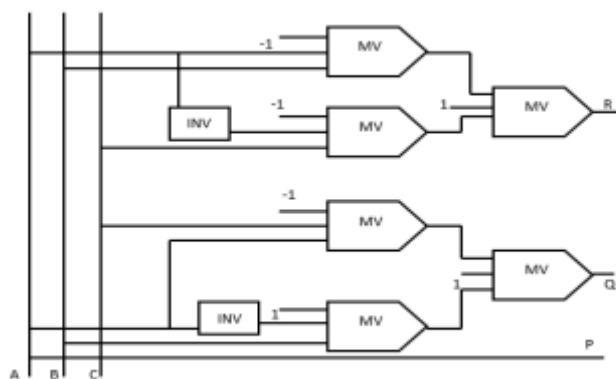


Table 4. Truth Table of Feynman Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	1	1

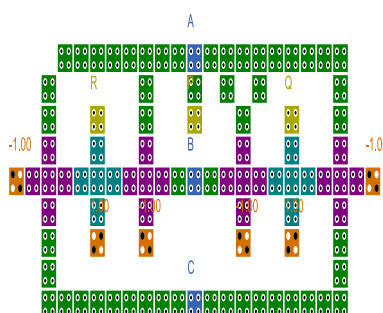


Fig. 15. Fredkin Gate in QCA Designer

IMPLEMENTATION OF ODD-PARITY GENERATOR

Let the information sources A, B, and C be the three bits of a message that must be sent through the medium. Px is the parity bit. The parity bit Px is shaped to such an extent that the all out number of 1's in the message gets odd (counting Px). The logic articulation of the three-piece odd-parity generator can be composed as.

$$P_x = A \oplus B \oplus C.$$

The truth table is shown in Table 5. From the truth table, Odd Parity bit Px refers to equality checking modes, where each arrangement of transmitted bits has an odd number of bits. In the event that the all out number of ones in the information in addition to the equality bit is an odd number of ones, it is called odd equality. On the off chance that the information as of now has an odd number of ones, the estimation of the additional equality bit is 0. We need to make utilization of two FG gate followed by the not gate to generate parity bit Px. Px composed of one exor operation pursued by exnor operation.



Fig.16. Block Diagram of Fredkin Gate

Table 5. Truth Table of Odd Parity Generator

Message Bits			Parity Bits
A	B	C	
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



Fig. 17. Odd parity Generator in QCA Designer

[illegible][illegible]

Timing diagram for the 74VHC04 hex inverters. The diagram shows 16 input signals (A through P) and their corresponding inverted outputs. The inputs are square waves with varying frequencies and duty cycles. The outputs are inverted square waves. The diagram is labeled "74VHC04" and "hex inverters".

<http://mkct.org.in/icmrd/>

V. POWER ANALYSIS

The electrons travel from one position to other through its wave nature. The heat dissipation by each cell in a QCA circuit is proportionate. Subsequently, in an exhibit of comparative QCcells, the all out scattered power can be assessed by totaling the dispersed intensity of all QCA cells inside the exhibit. The power utilization by the QCA circuit is reliant on the logic gates utilized in structuring the circuit. The power is calculated by making use of hamming distance. The instance of the inverter, 0 to 0 or 1 to 1 information exchanging implies Hamming separation '0', and the inverter has 0.8 meV disseminated power at $\gamma_i=0.2$ Energy and 8 meV at $\gamma_i=1.0$ Energy. For 0 to1 or 1 to 0 information exchanging, Hamming separation '1' is considered for the inverter and afterward dissemination will be 28.2 meV at $\gamma_i=0.2$ Energy and 30.3 meV at $\gamma_i=1.0$ Energy. A most extreme Hamming separation of '3' is considered for the majority voter for 000 to 111 input exchanging, which causes the most extreme disseminated vitality of 41 meV by the majority voter. Similarly, we can calculate power calculation of Odd parity generator which make utilization of two FG gate and one inverter. The FG gate require three majority voter and two not gate. The calculated power for FG gate is 104 meV at $\gamma_i=0.2$ Energy and 205 meV for Reversible odd Parity generator circuit.



Fig 22.1 and 22.2 Comparison of Area and Cost of Odd parity Generator in Various paper

VI. CONCLUSION

Reversible technology is very promising. In this paper, the reversible gates Fredkin and Tofoli are implemented using open source simulator QCA Designer and verify the simulation results. Further, the area and power parameters are analyzed for parity generator. The proposed design is compared with the available parity generator circuits. It is concluded that the area and power values are less in case of proposed design.

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